IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Chung Wai Leung et al.		
Assignee:	Mosel Vitelic, Inc.		
Title:	Nonvolatile Memory Structures and Fabrication Methods		
Application No.:	Unknown	Filing Date:	Herewith
Examiner:	Unknown	Group Art Unit:	Unknown
Docket No.:	M-11467-2D US		

San Jose, California
October 20, 2003

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR § 1.97(b)

Dear Sir:

Pursuant to 37 CFR § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying form PTO-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are not enclosed as all documents were previously cited by or submitted to the Patent Office in prior applications relied upon for priority under 35 U.S.C. 120(37 C.F.R. § 1.98(d)). The prior applications are U.S. Application No. 10/200,443, filed July 22, 2002, and U.S. Application No. 09/969,841 filed October 2, 2001.

Citation of these documents shall not be construed as:

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2. a representation that a search has been made, other than as described above; or

3. an admission that the information cited herein is, or is considered to be material to patentability as defined in § 1.56(b).

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Respectfully submitted,

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U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Serial No.
	M-11467-2D US	Unassigned
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	
(Use several sheets if necessary)	Leung et al.	
	Filing Date	Group
	Filed Herewith	Unassigned

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	4,794,565	12/27/1988	Wu et al.			
	AB	5,029,130	7/2/1991	Yeh			
	AC	5,045,488	9/3/1991	Yeh			
	AD	5,067,108	11/19/1991	Jenq			
	AE	5,120,671	6/9/1992	Tang, et al.			
	AF	5,202,850	4/13/1993	Jenq			
	AG	5,212,541	5/18/1993	Bergemont			
	AH	5,217,920	6/8/1993	Mattox, et al.			
	AI	5,242,848	9/7/1993	Yeh			
	AJ	5,264,387	11/23/1993	Beyer et al.			
	AK	5,278,087	1/11/1994	Jenq			
	AL	5,376,571	Dec-94	Bryant et al.			
	AM	5,631,179	May-97	Sung et al.			
	AN	5,741,719	Apr-98	Kim, Keon-soo			
	AO	5,783,471	Jul-98	Chu, Sam			
	AP	5,821,143	10/13/1998	Kim et al.			
	AQ	5,851,879	12/22/1998	Lin, et al.			
	AR	5,856,943	1/5/1999	Jeng			
	AS	5,909,628	6/1/1999	Chatterjee et al.			
	AT	5,912,843	6/15/1999	Jeng			
	AU	5,943,261	8/24/1999	Lee			
	AV	5,953,255	9/14/1999	Lee			
	AW	5,965,913	10/12/1999	Yuan, et al.			
	AX	5,977,584	11/2/1999	Kim			
	AY	6,001,706	12/14/1999	Tan, et al.			
	AZ	6,013,551	1/11/2000	Chen et al.			

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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U.S. Patent Documents

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	BA	6,043,536	3/28/2000	Numata et al.			
	BB	6,054,355	4/25/2000	Inumiya et al.			
	BC	6,057,572	5/2/2000	Ito et al.			
	BD	6,087,208	7/11/2000	Krivokapic et al.			
	BE	6,103,592	8/15/2000	Levy et al.			
	BF	6,165,692	12/26/2000	Kanai et al.			
	BG	6,166,415	12/26/2000	Sakemi et al.			
	BH	6,169,012	1/2/2001	Chen et al.			
	BI	6,171,910	1/9/2001	Hobbs et al.			
	BJ	6,171,971	1/9/2001	Natzle			
	BK	6,171,976	1/9/2001	Cheng			
	BL	6,177,303	1/23/2001	Schmitz et al.			
	BM	6,191,001	2/20/2001	Chen et al.			
	BN	6,191,049	2/20/2001	Song			
	BO	6,191,444	2/20/2001	Clampitt et al.			
	BP	6,355,524	Mar-02	Tuan et al.			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	BQ	*S. Aritome, S. Satoch, T. Maruyama, H. Watanabe, S. Shuto, G.J. Hemink, R. Shirota, S. Watanabe and F. Masuoka*, "A 0.67 mn^2 Self-Aligned Shallow Trench Isolation Cell (SA-STI Cell) For 3V – only 256Mbit Nand EEPROMs", (IEDM Tech. Dig. Dec. 11-14, 1994, PP. 61-64), pp. 3.6.1 - 3.6.4.
	BR	*William D. Brown, Joe E. Brewer,* "Nonvolatile Semiconductor Memory Technology" "A Comprehensive Guide to Understanding and Using NVSM Devices", (IEEE Press series on microelectronic systems 1998), pp. 21-23.
	BS	*Rebecca Mih et al.*, "0.18um Modular Triple Self-Aligned Embedded Split-Gate Flash Memory", 2000 Symposium on VLSI Technology, Digest of Technical Papers.
	BT	*K. Naruke, S. Yamada, E. Obi, S. Taguchi, and M. Wada*, "A New Flash-Erase EEProm Cell With A Sidewall Select-Gate On Its Source Side", (IEDM Tech. Dig. Dec. 3-6, 1989, PP, 603-606), pp. 25.7.1-25.7.4.

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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)				
	BU	*K. Shimizu, K. Narita, H. Watanabe, E. Kamiya, Y. Takeuchi, T. Yaegashi, S. Aritome, and T. Watanabe*, "A Novel High-Density $5F^2$ NAND STI Cell Technology Suitable for 256Mbit and 1 Gbit Flash Memories", (IEEE Tech. Dig. Dec. 7-10, 1997, pp. 271-274), pp. 11.1.1-11.1.4.		
	BV	*Riichiro Shirota*, "A Review of 256Mbit NAND Flash Memories and NAND Flash Future Trend", (Microelectronics Engineering Laboratory), unknown date before August 15, 2000, pp. 22-31.		
	BW	*A.T. Wu, T.Y. Chan, P.K. Ko and C. Hu*, "A Novel High-Speed, 5-Volt Programming Eprom Structure With Source-Side Injection", (IEDM Tech. Dig., pp. 584-587, 1986), pp. 108 - 111.		
Examiner			Date Considered	

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